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10/713,776	11/13/2003	Alok Kumar	10559-878001 / P17397	8759

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EXAMINER	
SAVLA, ARPAN P	

ART UNIT	PAPER NUMBER
2185	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PATDOCTC@fr.com

Office Action Summary	Application No.	Applicant(s)	
	10/713,776	KUMAR, ALOK	
	Examiner	Art Unit	
	Arpan P. Savla	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 October 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-11,13-21,23,24,26,27 and 29-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-11,13-21,23,24,26,27 and 29-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

This Office action is in response to Applicant's communication filed October 28, 2008 in response to the Office action dated August 29, 2008. Claims 1, 4, 5, 11, 14, 15, 21, 24, 27, and 30 have been amended. Claims 2, 12, 22, 25, and 28 have been canceled. Claims 1, 3-11, 13-21, 23, 24, 26, 27, 29, and 30-37 are pending in this application.

OBJECTIONS

Specification

1. In view of Applicant's amendment, the objection to the specification is withdrawn.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 3-11, 13-21, 23, 24, 26, 27, 29, and 30-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wong et al. (U.S. Patent 5,701,432) (hereinafter "Wong") in view of Bergantino et al. (U.S. Patent 6,826,180) (hereinafter "Bergantino").

4. **As per claims 1 and 11**, Wong discloses a method comprising:

allocating a memory entry in a memory device included in a multithreaded engine to executable instructions stored in the multithreaded engine, the executable instructions to be executed on the multithreaded engine (col. 3, lines 7-9; col. 4, lines 53-54; col. 5, lines 10-15; Figs. 1 and 2); *It should be noted that computer program product in claims 11-20 executes the same functions as the methods in claims 1-10. Therefore, any reference(s) that teach claims 1-10 also teach the corresponding claims 11-20. It should also be noted that the "multi-threaded processing system" of Fig. 1 is analogous to the "multithreaded engine."*

including a unique identifier assigned to the executable instructions in a portion of the memory entry (col. 5, lines 18-19; col. 7, lines 54-57; Fig. 2, element 203); *It should be noted that "key 203" is analogous to the "unique identifier."*

and maintaining a count of a number of threads included in the multithreaded engine that use the memory entry when the multithreaded engine executes the executable instructions (col. 5, lines 18-20 and 53-61; Fig. 2, element 211).

Wong does not disclose a packet processor.

Bergantino discloses a packet processor (Fig. 1, element 100).

Wong and Bergantino are analogous art because they are from the same field of endeavor, that being data processing systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Wong's multi-threaded processing system within Bergantino's packet processor. The motivation for doing so would have been to allow

multi-threaded processing of packets in a networking environment, thus speeding up of the overall system throughput in the networking environment.

5. **As per claim 21**, Wong discloses a memory manager comprising:

a system to:

allocate a memory entry in a memory device included in a multithreaded engine to executable instructions stored in the multithreaded engine, the executable instructions to be executed on the multithreaded engine (col. 3, lines 7-9; col. 4, lines 53-54; col. 5, lines 10-15; Figs. 1 and 2);

include a unique identifier assigned to the executable instructions in a portion of the memory entry (col. 5, lines 18-19; col. 7, lines 54-57; Fig. 2, element 203);

maintain a count of a number of threads included in the multithreaded engine that use the memory entry when the multithreaded engine executes the executable instructions (col. 5, lines 18-20 and 53-61; Fig. 2, element 211);

determine the memory entry is no longer being used by a thread in the multithreaded engine (col. 5, lines 55-56);

and decrement the count (col. 5, lines 56-57).

Wong does not disclose a packet processor.

Bergantino discloses a packet processor (Fig. 1, element 100).

Wong and Bergantino are analogous art because they are from the same field of endeavor, that being data processing systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Wong's multi-threaded processing system within

Bergantino's packet processor. The motivation for doing so would have been to allow multi-threaded processing of packets in a networking environment, thus speeding up of the overall system throughput in the networking environment.

6. **As per claim 24**, Wong discloses a system comprising:

a system to:

allocate a memory entry in a memory device included in a multithreaded engine to executable instructions stored in the multithreaded engine, the executable instructions to be executed on the multithreaded engine (col. 3, lines 7-9; col. 4, lines 53-54; col. 5, lines 10-15; Figs. 1 and 2);

include a unique identifier assigned to the executable instructions in a portion of the memory entry (col. 5, lines 18-19; col. 7, lines 54-57; Fig. 2, element 203);

maintain a count of a number of threads included in the multithreaded engine that use the memory entry when the multithreaded engine executes the executable instructions (col. 5, lines 18-20 and 53-61; Fig. 2, element 211);

determine the initiation of use of the memory entry by a thread included in the multithreaded engine (col. 5, lines 54-55);

and in response to the determining, increment the count (col. 5, lines 54-55).

Wong does not disclose a packet processor.

Bergantino discloses a packet processor (Fig. 1, element 100).

Wong and Bergantino are analogous art because they are from the same field of endeavor, that being data processing systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Wong's multi-threaded processing system within Bergantino's packet processor. The motivation for doing so would have been to allow multi-threaded processing of packets in a networking environment, thus speeding up of the overall system throughput in the networking environment.

7. **As per claim 27**, Wong discloses a device comprising:

a system to:

allocate a memory entry in a memory device included in a multithreaded engine to executable instructions stored in the multithreaded engine, the executable instructions to be executed on the multithreaded engine (col. 3, lines 7-9; col. 4, lines 53-54; col. 5, lines 10-15; Figs. 1 and 2);

include a unique identifier assigned to the executable instructions in a portion of the memory entry (col. 5, lines 18-19; col. 7, lines 54-57; Fig. 2, element 203);

maintain a count of a number of threads included in the multithreaded engine that use the memory entry when the multithreaded engine executes the executable instructions (col. 5, lines 18-20 and 53-61; Fig. 2, element 211);

Wong does not disclose an input port for receiving packets;

an output for delivering the received packets;

and a network processor.

Bergantino discloses an input port for receiving packets (Fig. 1, element 101, signal 1);

an output for delivering the received packets (Fig. 1, element 101, signal 13);

and a network processor (Fig. 1, element 100).

Wong and Bergantino are analogous art because they are from the same field of endeavor, that being data processing systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Wong's multi-threaded processing system within Bergantino's packet processor. The motivation for doing so would have been to allow multi-threaded processing of packets in a networking environment, thus speeding up of the overall system throughput in the networking environment.

8. **As per claim 30**, Wong discloses a method comprising:

allocating a memory entry to an executable microblock to be executed on a multithreaded microengine, the memory entry and the executable microblock located in the multithreaded engine (col. 3, lines 7-9; col. 4, lines 53-54; col. 5, lines 10-15; Figs. 1 and 2);

and including a unique identifier assigned to the executable microblock in a portion of the memory entry (col. 5, lines 18-19; col. 7, lines 54-57; Fig. 2, element 203).

Wong does not disclose a 32-bit long content-addressable-memory (CAM) entry;

a network processor;

and a 4-bit long unique identifier.

Wong discloses a content-addressable-memory (CAM) entry (Fig. 1, element 106);

and a network processor (Fig. 1, element 100).

Wong and Bergantino are analogous art because they are from the same field of endeavor, that being data processing systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Wong's multi-threaded processing system within Bergantino's packet processor. The motivation for doing so would have been to allow multi-threaded processing of packets in a networking environment, thus speeding up of the overall system throughput in the networking environment.

The combination of Wong/Bergantino does not expressly disclose a 32-bit long content-addressable-memory (CAM) entry;

and a 4-bit long unique identifier.

However, neither Wong nor Bergantino precludes a 32-bit long memory entry or a 4-bit long unique identifier (i.e. key 203). In fact, it is well within the scope of both inventions to allow a 32-bit long memory entry and a 4-bit long key 203. Therefore, at the time of the invention it would have been obvious to a person of ordinary skill in the art to implement the memory entry as 32-bits long and implement the key 203 as 4-bits long as a matter of design choice. See *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), *cert. denied*, 469 U.S. 830, 225 USPQ 232 (1984), in which the Federal Circuit held that, where the only difference between the prior art and the claims was a recitation of relative dimensions of the claimed device and a device having the claimed relative dimensions would not perform differently than the prior art device, the claimed device was not patentably distinct from the prior art device.

9. **As per claims 3, 13, 23, 26, and 29**, the combination of Wong/Bergantino discloses maintaining a bit to represent availability of the memory entry for thread use (Wong, col. 5, lines 36-39).

10. **As per claims 4 and 14**, the combination of Wong/Bergantino discloses maintaining the count includes incrementing the count to represent a thread initiating use of the memory entry (Wong, col. 5, lines 54-55).

11. **As per claims 5 and 15**, the combination of Wong/Bergantino discloses maintaining the count includes decrementing the count to represent a thread halting use of the memory entry (col. 5, lines 55-57).

12. **As per claims 6 and 16**, the combination of Wong/Bergantino discloses maintaining the bit includes clearing the bit to represent availability of the memory entry for thread use (Wong, col. 5, lines 36-39).

However, active high (1) and active low (0) are art-recognized equivalents in the computer arts insomuch as it is immaterial whether a state bit is high (setting the bit) or low (clearing the bit) in one state so long as the bit is the opposite level in the opposite state. Therefore, at the time of the invention it would have been obvious to a person of ordinary skill in the art to substitute Wong's entry lock being cleared when the entry is available with an entry lock that is instead set when the entry is available.

13. **As per claims 7 and 17**, the combination of Wong/Bergantino discloses maintaining the bit includes setting the bit to represent unavailability of the memory entry for thread use (Wong, col. 5, lines 36-39).

However, active high (1) and active low (0) are art-recognized equivalents in the computer arts insomuch as it is immaterial whether a state bit is high (setting the bit) or low (clearing the bit) in one state so long as the bit is the opposite level in the opposite state. Therefore, at the time of the invention it would have been obvious to a person of ordinary skill in the art to substitute Wong's entry lock being set when the entry is unavailable with an entry lock that is instead cleared when the entry is unavailable.

14. **As per claims 8 and 18**, the combination of Wong/Bergantino discloses checking the bit to determine the availability of the memory entry for thread use (Wong, col. 5, lines 36-39).

15. **As per claims 9 and 19**, see the rejection of claim 30 above.

16. **As per claims 10 and 20**, the combination of Wong/Bergantino discloses the memory entry identifies a location in a local memory included in the multithreaded engine of the packet processor (Wong, col. 5, lines 23-25; Fig. 2, element 205; Bergantino, Fig. 1, element 100).

17. **As per claim 31**, the combination of Wong/Bergantino discloses maintaining a count of threads included in the multithreaded microengine that use the CAM entry (Wong, col. 5, lines 18-20 and 53-61; Fig. 2, element 211; Bergantino, Fig. 1, element 106).

18. **As per claim 32**, the combination of Wong/Bergantino discloses maintaining a bit in a status register to represent availability of the CAM entry to identify a local memory location (Wong, col. 5, lines 36-39; Bergantino, Fig. 1, element 106).

19. **As per claims 33-37**, the combination of Wong/Bergantino discloses the memory entry comprises a content-addressable memory entry (Bergantino, Fig. 1, element 106).

Response to Arguments

20. Applicant's arguments with respect to **claims 1, 3-11, 13-21, 23, 24, 26, 27, 29, and 30-37** have been considered but are moot in view of the new grounds of rejection above.

Conclusion

STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by MPEP 707.70(i):

CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, **claims 1, 3-11, 13-21, 23, 24, 26, 27, 29, and 30-37** have received an action on the merits and are subject of a final action.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arpan P. Savla whose telephone number is (571) 272-1077. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on (571) 272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Arpan Savla/
Examiner, Art Unit 2185
June 8, 2009

/Sanjiv Shah/
Supervisory Patent Examiner, Art Unit 2185